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**In the claims:**

The listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A transistor comprising a source contact, a drain contact and a gate contact and a channel region between the source and drain contacts at least a portion of which comprises a hybrid layer comprising semiconductor material, wherein the transistor comprises a current aperture transistor and wherein a portion of the channel region through the current aperture comprises a vertical portion and a horizontal portion.

2. (Cancelled).

3. (Currently Amended) The transistor of Claim [[2]] 1, wherein the hybrid layer comprising semiconductor material comprises a Group III-nitride semiconductor material.

4. (Currently Amended) The transistor of Claim [[2]] 1, wherein the hybrid layer comprising semiconductor material comprises a region comprising p-type or insulating semiconductor material and a lateral region comprising n-type semiconductor material.

5. (Cancelled).

6. (Original) The transistor of Claim 1, wherein the hybrid layer comprises a pendeo-epitaxial layer having a higher doping level in laterally grown portions of the pendeo-epitaxial layer.

7. (Original) The transistor of Claim 1, wherein the hybrid layer comprises a epitaxial laterally overgrown layer having a higher doping level in the laterally grown portions of the epitaxial laterally overgrown layer.

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8. (Currently Amended) ~~The transistor of Claim 1, further comprising:~~ A transistor comprising a source contact, a drain contact and a gate contact and a channel region between the source and drain contacts at least a portion of which comprises a hybrid layer comprising semiconductor material:

a first n-type nitride-based layer on a substrate, the first n-type nitride-based layer having a first surface opposite the substrate and having an aperture having a sidewall;

a nitride-based layer on the first n-type nitride-based layer and extending onto the sidewall of the aperture, where a portion of the nitride-based layer on the sidewall of the aperture is n-type and a portion of the nitride-based layer on the first surface of the first n-type nitride-based layer is p-type and/or insulating;

an unintentionally doped nitride-based layer on the nitride based layer and extending to substantially fill the aperture, the unintentionally doped nitride-based layer having a portion of n-type nitride-based semiconductor material on the n-type portion of the nitride-based layer;

first and second layers of nitride-based semiconductor material on the unintentionally doped nitride-based layer and configured to provide a two-dimensional electron gas (2DEG) in a region of an interface between the first and second semiconductor material layers; and

wherein the source contact and the gate contact are provided on the second layer comprising nitride-based semiconductor material and the drain contact is electrically connected to the first n-type nitride-based layer.

9. (Original) The transistor of Claim 8, wherein the substrate has a trench formed therein and wherein the first n-type nitride-based layer, the nitride based layer and the unintentionally doped nitride-based layer are cantilevered over the trench.

10. (Original) The transistor of Claim 9, further comprising a second n-type nitride-based layer disposed between the first n-type nitride-based layer and the substrate, wherein the second n-type nitride based layer extends onto sidewalls and a floor of the trench.

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11. (Withdrawn) The transistor of Claim 8, further comprising a mask region on the substrate and wherein the first n-type nitride-based layer, the nitride based layer and the unintentionally doped nitride-based layer extend onto the mask region.

12. (Withdrawn) The transistor of Claim 11, further comprising a second n-type nitride-based layer disposed between the substrate and the first n-type nitride based layer and wherein the mask region is on the second n-type nitride-based layer.

13. (Withdrawn) The transistor of Claim 12, further comprising a third n-type nitride-based layer between the second nitride-based layer and the substrate.

14. (Original) The transistor of Claim 8, wherein the substrate comprises a silicon carbide substrate and wherein the drain contact is provided on the substrate opposite the first n-type nitride-based layer.

15. (Original) The transistor of Claim 8, wherein the substrate comprises a gallium nitride substrate.

16. (Original) The transistor of Claim 8, further comprising an insulating layer between the gate contact and the second layer.

17. (Original) The transistor of Claim 8, wherein the first n-type nitride-based layer comprises a GaN based layer, the nitride-based layer on the second n-type nitride-based layer comprises a GaN based layer, the unintentionally doped nitride-based layer comprises a GaN based layer, the first layer comprises an unintentionally doped GaN based layer and the second layer comprises an AlGaN and/or InAlN based layer.

18. (Original) A transistor comprising:  
a substrate having a trench therein;  
a first pendeo-epitaxial layer comprising semiconductor material of the substrate and having spaced apart cantilevered portions that extend over the trench;

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a second pendeo-epitaxial layer comprising semiconductor material of a second conductivity type and/or insulating on the first pendeo-epitaxial layer comprising semiconductor material and that includes spaced apart portions that extend from end surfaces of the cantilevered portions of the first pendeo-epitaxial layer that are the first conductivity type;

a third pendeo-epitaxial layer comprising unintentionally doped semiconductor material on the second pendeo-epitaxial layer and that includes portions that extend from the spaced apart portions and coalesce and are the first conductivity type;

a channel layer comprising semiconductor material on the third pendeo-epitaxial layer;

a barrier layer on the channel layer;

a source contact on the barrier layer;

a gate contact on the barrier layer; and

a drain contact electrically connected to the first layer comprising conformal semiconductor material.

19. (Original) The transistor of Claim 18, further comprising a first layer comprising conformal semiconductor material of a first conductivity type on the substrate and the trench and disposed between the substrate and the first pendeo-epitaxial layer;

20. (Original) The transistor of Claim 18, wherein the first conductivity type is n-type and the second conductivity type is p-type.

21. (Original) The transistor of Claim 18, wherein the semiconductor material comprises a nitride-based semiconductor material.

22. (Original) The transistor of Claim 21, wherein the substrate comprises silicon carbide.

23. (Original) The transistor of Claim 21, wherein the substrate comprises gallium nitride.

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24. (Original) The transistor of Claim 22, wherein the silicon carbide substrate is the first conductivity type and wherein the drain contact is provided on the silicon carbide substrate.

25. (Original) The transistor of Claim 21, wherein the nitride-based semiconductor material comprises a GaN based semiconductor material.

26-45. (Cancelled).

46. (Currently Amended) A method of fabricating a transistor comprising:  
forming a channel region at least a portion of which comprises a hybrid layer comprising semiconductor material; and  
forming a source contact, a drain contact and a gate contact, wherein the channel region is between the source and drain contacts, wherein the transistor comprises a current aperture transistor and wherein a portion of the channel region through the current aperture comprises a vertical portion and a horizontal portion.

47. (Original) The method of Claim 46, wherein the hybrid layer comprising semiconductor material comprises a Group III-nitride semiconductor material.

48. (Original) The method of Claim 46, wherein forming a channel region at least a portion of which comprises a hybrid layer comprising semiconductor material comprises forming a hybrid layer comprising a region comprising p-type or insulating semiconductor material and a region comprising n-type semiconductor material.

49. (Cancelled).

50. (Original) The method of Claim 46, wherein forming a channel region between the source and drain contacts at least a portion of which comprises a hybrid layer

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comprising semiconductor material comprises pendeo-epitaxially growing a layer having a higher doping level in the laterally grown portions of the pendeo-epitaxial layer.

51. (Original) The method of Claim 46, wherein forming a channel region between the source and drain contacts at least a portion of which comprises a hybrid layer comprising semiconductor material comprises forming a layer using epitaxial lateral overgrowth, the epitaxial laterally overgrown layer having a higher doping level in the laterally grown portions of the epitaxial laterally overgrown layer.

52. (Currently Amended) ~~The method of Claim 46,~~ A method of fabricating a transistor comprising:

forming a channel region at least a portion of which comprises a hybrid layer comprising semiconductor material; and

forming a source contact, a drain contact and a gate contact, wherein the channel region is between the source and drain contacts, wherein forming a channel region at least a portion of which comprises a hybrid layer comprising semiconductor material further comprises:

forming a first n-type nitride-based layer on a substrate, the first n-type nitride-based layer having a first surface opposite the substrate and an aperture having sidewalls;

forming a nitride-based layer on the first n-type nitride-based layer and extending onto the sidewalls of the aperture, where a portion of the nitride-based layer on the sidewalls of the aperture is n-type and a portion of the nitride-based layer on the first surface of the first n-type nitride-based layer is p-type and/or insulating;

forming an unintentionally doped nitride-based layer on the nitride based layer and extending to substantially fill the aperture, the unintentionally doped nitride-based layer having portions of n-type nitride-based semiconductor material on the n-type portions of the nitride-based layer;

forming first and second layers of nitride-based semiconductor material on the unintentionally doped nitride-based layer and configured to provide a two-dimensional electron gas (2DEG) in a region of an interface between the first and second semiconductor material layers; and

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wherein the source contact and the gate contact are formed on the second layer comprising nitride-based semiconductor material and the drain contact is electrically connected to the first n-type nitride-based layer.

53. (Original) The method of Claim 52, further comprising:

forming a trench in the substrate; and

wherein forming the first n-type nitride-based layer, forming the nitride based layer and forming the unintentionally doped nitride-based layer comprise:

pendeo-epitaxially growing the first n-type nitride-based layer to be cantilevered over the trench;

pendeo-epitaxially growing the nitride-based layer to be cantilevered over the trench; and

pendeo-epitaxially growing the unintentionally doped nitride-based layer to be cantilevered over the trench.

54. (Original) The method of Claim 53, further comprising forming a second n-type nitride-based layer on the substrate and extending into the trench and wherein forming a first n-type nitride-based layer on the substrate comprises forming a first n-type nitride-based layer on the second n-type nitride-based layer.

55. (Withdrawn) The method of Claim 52, further comprising:

forming a mask region on the substrate; and

wherein forming the first n-type nitride-based layer, forming the nitride based layer and forming the unintentionally doped nitride-based layer comprises:

forming the first n-type nitride-based layer utilizing epitaxial lateral overgrowth such that a portion of the first n-type nitride-based layer extends over the mask region;

forming the nitride based layer utilizing epitaxial lateral overgrowth such that a portion of the nitride-based layer extends over the mask region; and

forming the unintentionally doped nitride-based layer utilizing epitaxial lateral overgrowth such that a portion of the unintentionally doped nitride-based layer extends over the mask region.

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56. (Withdrawn) The method of Claim 55, further comprising forming a second n-type nitride-based layer on the substrate, wherein forming a mask region on the substrate comprises forming a mask region on the second n-type nitride-based layer and wherein forming a first n-type nitride-based layer on the substrate comprises forming a first n-type nitride-based layer on the second n-type nitride-based layer.

57. (Withdrawn) The method of Claim 56, further comprising forming a third n-type nitride-based layer between the second nitride-based layer and the substrate.

58. (Original) The method of Claim 52, wherein the substrate comprises a silicon carbide substrate and wherein the drain contact is provided on the substrate.

59. (Original) The method of Claim 52, further comprising forming an insulating layer between the gate contact and the second layer.

60. (Original) The method of Claim 52, wherein the first n-type nitride-based layer comprises a GaN based layer, the nitride-based layer on the second n-type nitride-based layer comprises a GaN based layer, the unintentionally doped nitride-based layer comprises a GaN based layer, the first layer comprises an unintentionally doped GaN based layer and the second layer comprises an AlGaN and/or InAlN based layer.

61. (Currently Amended) A method of fabricating a transistor comprising:  
forming a trench in a substrate;  
forming a first pendeo-epitaxial layer comprising semiconductor material of a first conductivity type by pendeo-epitaxial growth on the substrate and having spaced apart cantilevered portions that extend over the trench;  
forming a second pendeo-epitaxial layer comprising semiconductor material of a second conductivity type and/or insulating by pendeo-epitaxial growth on the first pendeo-epitaxial layer comprising semiconductor material and that includes spaced apart portions

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that extend from end surfaces of the cantilevered portions of the first pendeo-epitaxial layer that are the first conductivity type;

forming a third pendeo-epitaxial layer comprising unintentionally doped semiconductor material by pendeo-epitaxial growth on the second pendeo-epitaxial layer and that includes portions that extend from the spaced apart portions and coalesce and are the first conductivity type;

forming a channel layer comprising semiconductor material on the third pendeo-epitaxial layer;

forming a barrier layer on the channel layer;

forming a source contact on the barrier layer;

forming a gate contact on the barrier layer; and

forming a drain contact electrically connected to ~~[[the]]~~ a first conformal layer comprising semiconductor material.

62. (Original) The method of Claim 61, further comprising forming a first layer comprising conformal semiconductor material of a first conductivity type on the substrate and the trench and wherein forming a first pendeo-epitaxial layer comprises forming a first pendeo-epitaxial layer on the first layer.

63. (Original) The method of Claim 61, wherein the first conductivity type is n-type and the second conductivity type is p-type.

64. (Original) The method of Claim 61, wherein the semiconductor material comprises a nitride-based semiconductor material.

65. (Original) The method of Claim 64, wherein the substrate comprises gallium nitride.

66. (Original) The method of Claim 64, wherein the substrate comprises silicon carbide.

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67. (Original) The method of Claim 66, wherein the silicon carbide substrate is the first conductivity type and wherein forming the drain contact comprises forming the drain contact on the silicon carbide substrate.

68. (Original) The method of Claim 64, wherein the nitride-based semiconductor material comprises a GaN based semiconductor material.

69-88. (Cancelled).